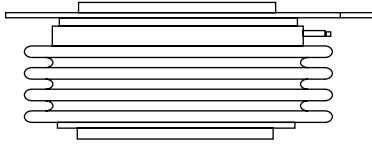


Inverter Grade Thyristors (Hockey PUK Version), 940 A



TO-200AC (B-PUK)

FEATURES

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- International standard case TO-200AC (B-PUK)
- High surge current capability
- Low thermal impedance
- High speed performance
- Lead (Pb)-free
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	940 A
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TYPICAL APPLICATIONS

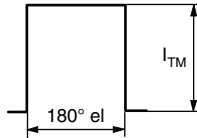
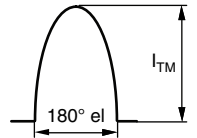
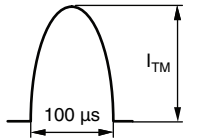
- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		940	A
	T_{hs}	55	°C
$I_{T(RMS)}$		1900	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	20 000	A
	60 Hz	20 950	
I^2t	50 Hz	2000	kA ² s
	60 Hz	1820	
V_{DRM}/V_{RRM}		400 to 800	V
t_q	Range	10 to 20	μs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS
VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V _{DRM} /V _{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I _{DRM} /I _{RRM} MAXIMUM AT T _J = T _J MAXIMUM mA
ST733C..L	04	400	500	75
	08	800	900	

CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	2200	1900	3580	3100	6800	5920	A
400 Hz	2050	1660	3600	3130	3750	3240	
1000 Hz	1370	1070	2900	2450	2120	1780	
2500 Hz	500	370	1220	980	960	770	
Recovery voltage V_R	50		50		50		V
Voltage before turn-on V_D	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/ μ s
Heatsink temperature	40	55	40	55	40	55	$^{\circ}$ C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		Ω/μ F

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			940 (350)	A
					55 (85)	$^{\circ}$ C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 $^{\circ}$ C heatsink temperature double side cooled			1900	A
Maximum peak, one half cycle, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	20 000	
		t = 8.3 ms			20 950	
		t = 10 ms	100 % V_{RRM} reappplied		16 800	
		t = 8.3 ms			17 600	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reappplied		2000	
		t = 8.3 ms			1820	
		t = 10 ms	100 % V_{RRM} reappplied		1410	
		t = 8.3 ms			1290	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reappplied			20 000	$kA^2\sqrt{s}$
Maximum peak on-state voltage	V_{TM}	$I_{TM} = 1700$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse			1.63	V
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			1.09	
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			1.20	
Low level value of forward slope resistance	r_{t1}	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.32	m Ω
High level value of forward slope resistance	r_{t2}	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.29	
Maximum holding current	I_H	$T_J = 25$ $^{\circ}$ C, $I_T > 30$ A			600	mA
Typical latching current	I_L	$T_J = 25$ $^{\circ}$ C, $V_A = 12$ V, $R_a = 6$ Ω , $I_G = 1$ A			1000	



SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$, $I_{TM} = 2 \times di/dt$ Gate pulse: 20 V 20 Ω , 10 μ s 0.5 μ s rise time	1000	A/ μ s
Typical delay time	t_d	$T_J = 25^\circ\text{C}$, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μ s Resistive load, gate pulse: 10 V, 5 Ω source	1.5	μ s
Maximum turn-off time	minimum	$T_J = T_J$ maximum, $I_{TM} = 550$ A, commutating $di/dt = 40$ A/ μ s $V_R = 50$ V, $t_p = 500$ μ s, dV/dt : see table in device code	10	
	maximum		20	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	75	mA

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	+ V_{GM}		20	
Maximum peak negative gate voltage	- V_{GM}		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25^\circ\text{C}$, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		- 40 to 125	$^\circ\text{C}$
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.073	K/W
		DC operation double side cooled	0.031	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.011	
		DC operation double side cooled	0.005	
Mounting force, ± 10 %			14 700 (1500)	N (kg)
Approximate weight			255	g
Case style		See dimensions - link at the end of datasheet	TO-200AC (B-PUK)	

ST733CLPbF Series



Vishay High Power Products Inverter Grade Thyristors
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ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.009	0.009	0.006	0.006	T _J = T _J maximum	K/W
120°	0.011	0.011	0.011	0.011		
90°	0.014	0.014	0.015	0.015		
60°	0.020	0.021	0.021	0.022		
30°	0.036	0.036	0.036	0.036		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

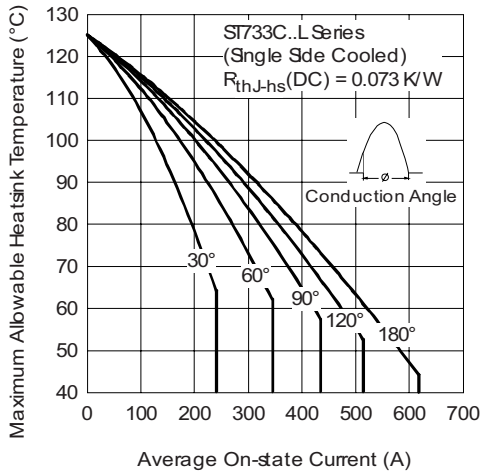


Fig. 1 - Current Ratings Characteristics

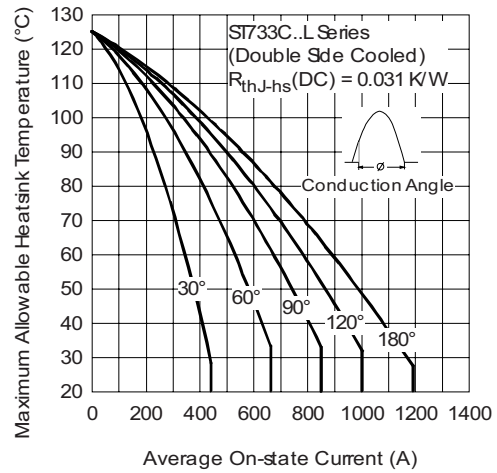


Fig. 3 - Current Ratings Characteristics

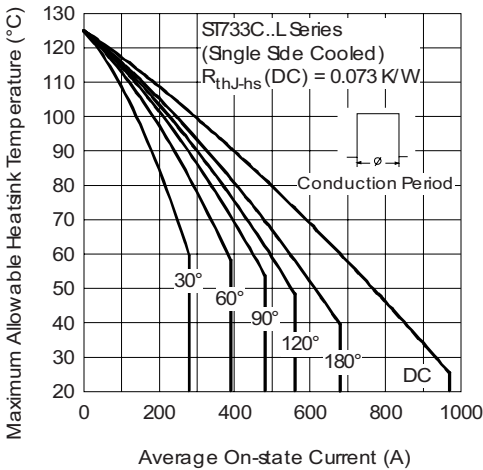


Fig. 2 - Current Ratings Characteristics

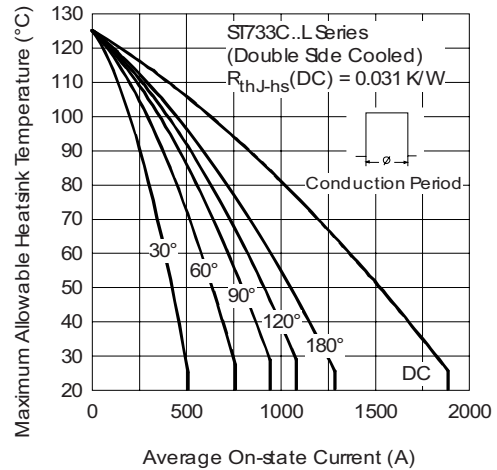


Fig. 4 - Current Ratings Characteristics

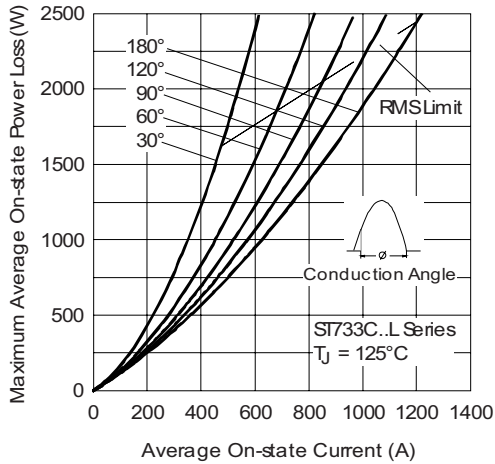


Fig. 5 - On-State Power Loss Characteristics

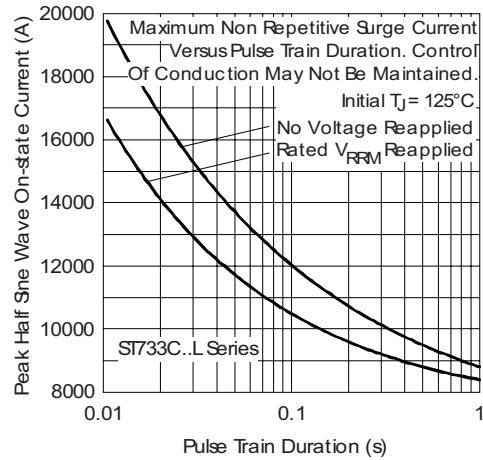


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

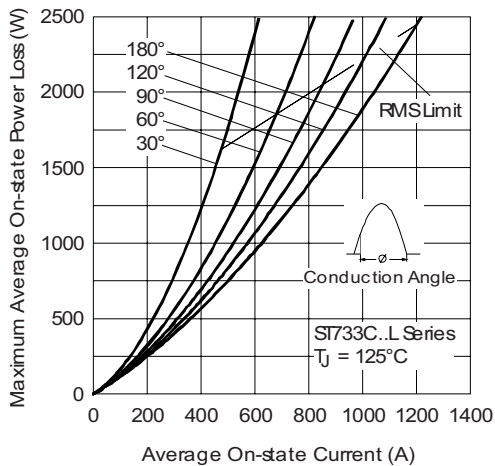


Fig. 6 - On-State Power Loss Characteristics

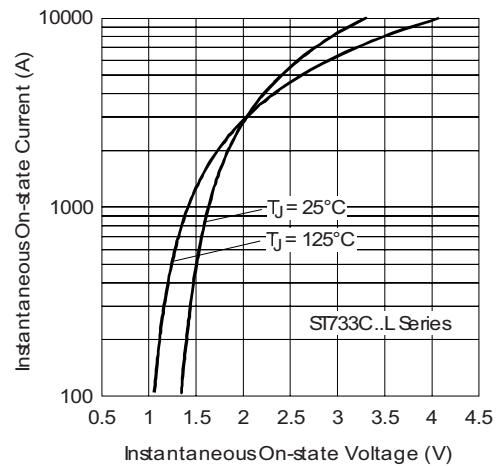


Fig. 9 - On-State Voltage Drop Characteristics

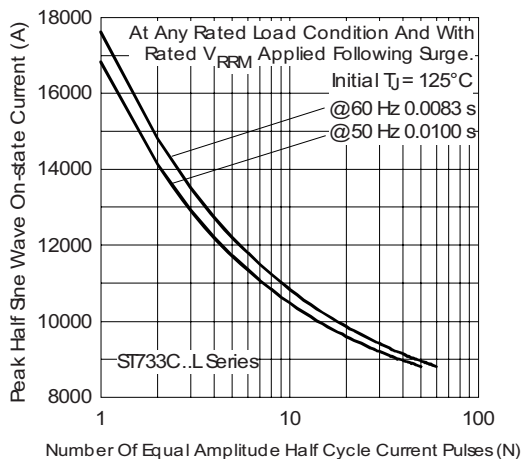


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

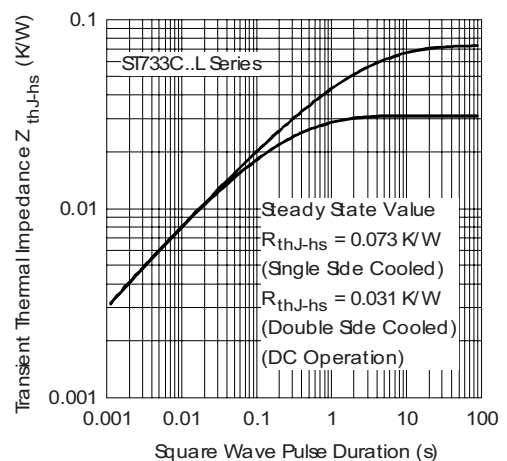


Fig. 10 - Thermal Impedance Z_{thJC} Characteristics

ST733CLPbF Series



Vishay High Power Products Inverter Grade Thyristors
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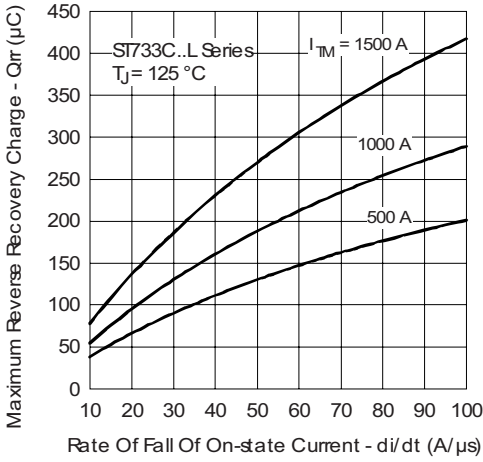


Fig. 11 - Reverse Recovered Charge Characteristics

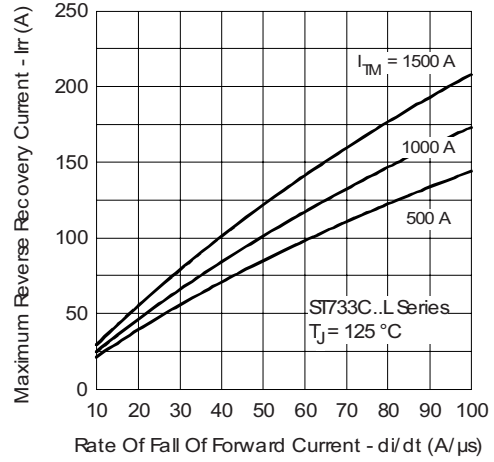


Fig. 12 - Reverse Recovered Current Characteristics

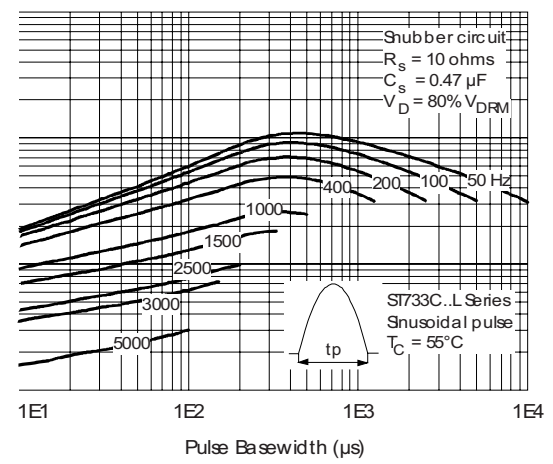
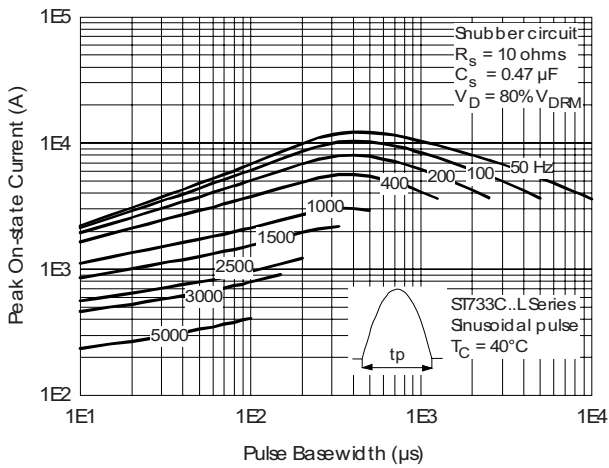


Fig. 13 - Frequency Characteristics

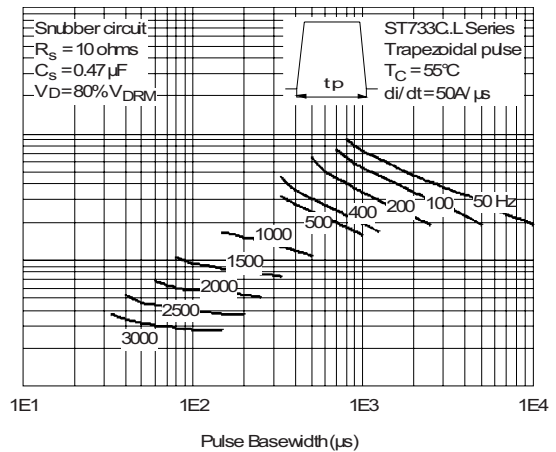
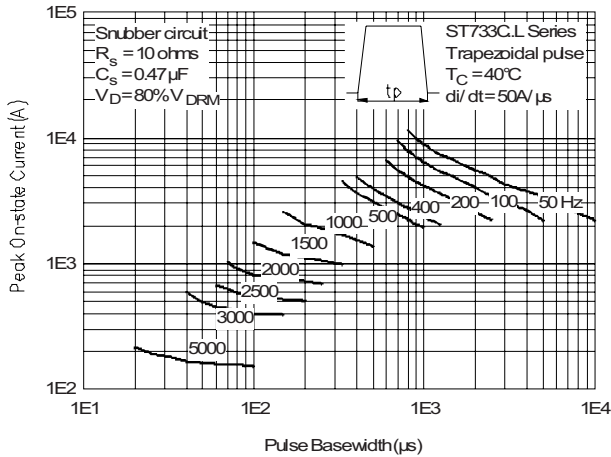


Fig. 14 - Frequency Characteristics

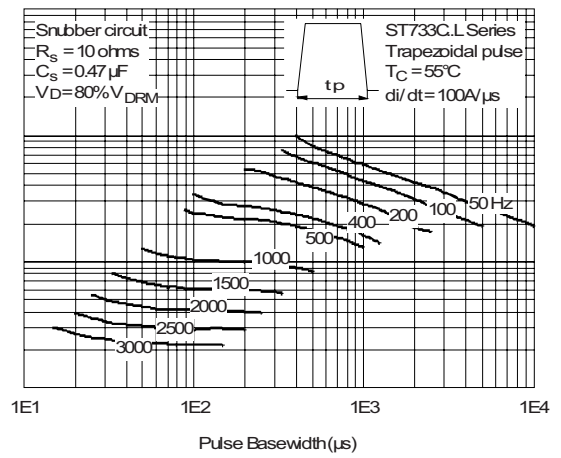
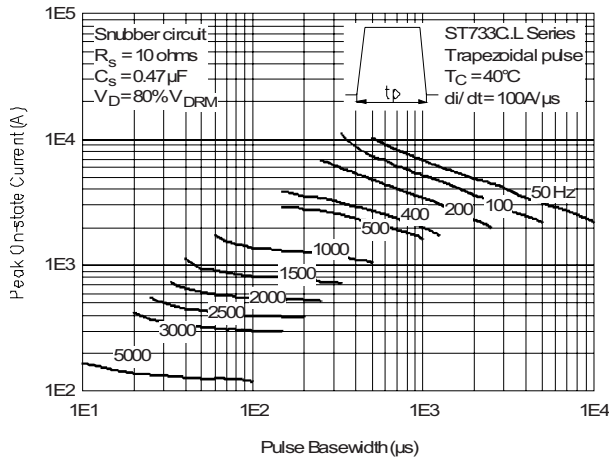


Fig. 15 - Frequency Characteristics

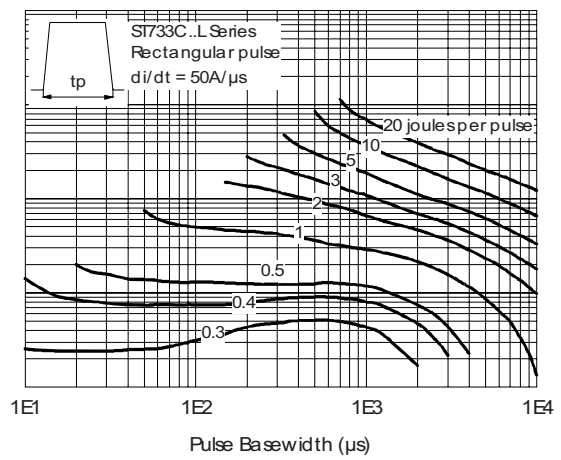
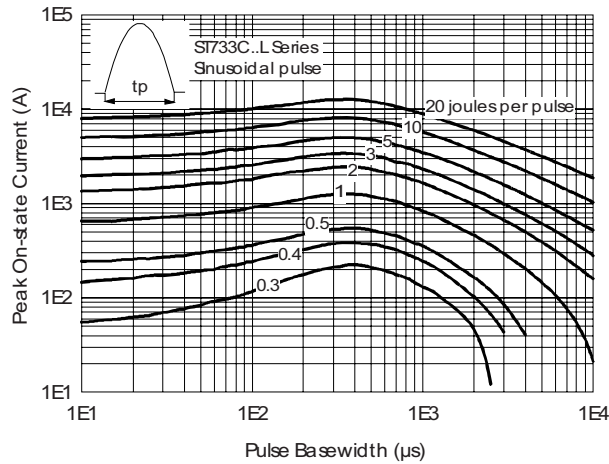


Fig. 16 - Maximum On-State Energy Power Loss Characteristics

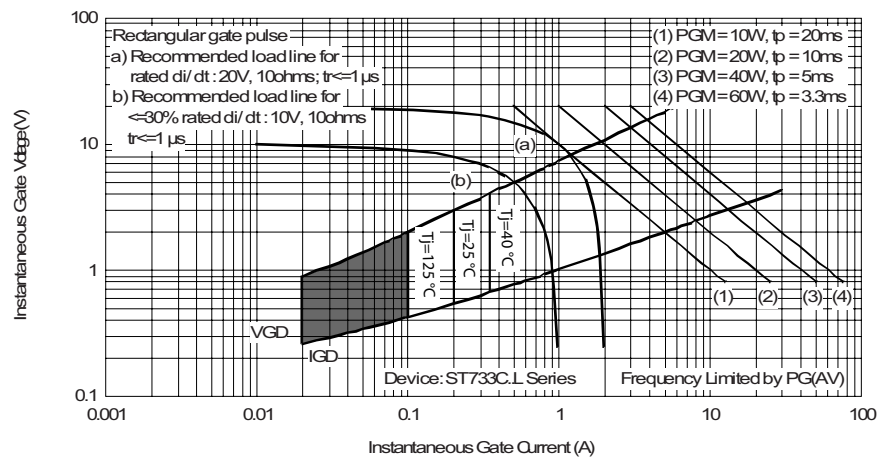


Fig. 17 - Gate Characteristics

ST733CLPbF Series



Vishay High Power Products Inverter Grade Thyristors
(Hockey PUK Version), 940 A

ORDERING INFORMATION TABLE

Device code	ST	73	3	C	08	L	H	K	1	-	P
	1	2	3	4	5	6	7	8	9	10	11

- 1** - Thyristor
- 2** - Essential part number
- 3** - 3 = Fast turn-off
- 4** - C = Ceramic PUK
- 5** - Voltage code x 100 = V_{RRM}
(see Voltage Ratings table)
- 6** - L = PUK case TO-200AC (B-PUK)
- 7** - Reapplied dV/dt code (for t_q test condition)
- 8** - t_q code
- 9** - 0 = Eyelet terminals
(gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals
(gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals
(gate and auxiliary cathode soldered leads)
3 = Fast-on terminals
(gate and auxiliary cathode soldered leads)
- 10** - Critical dV/dt:
 - None = 500 V/ μ s (standard value)
 - L = 1000 V/ μ s (special selection)
- 11** - P = Lead (Pb)-free

dV/dt - t_q combinations available						
	dV/dt (V/ μ s)	20	50	100	200	400
t_q (μ s)	10	CN	DN	EN	-	-
	12	CM	DM	EM	FM*	-
	15	CL	DL	EL	FL*	HL
	18	CP	DP	EP	FP	HP
	20	CK	DK	EK	FK	H

* Standard part number.
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95076



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